

SPECIFICATION FOR
TFT LCD MODULE

MODEL NO: RV133FHM-300-30

Accepted by: （接受部门）	
Signature（签字）	Date（日期）
Proposed by: Technical Service Division （技术服务部）	
Signature（签字）	Date（日期）

1.0 GENERAL DESCRIPTION.....	4
2.0 MECHANICAL SPECIFICATION.....	5
3.0 INPUT INTERFACE PIN ASSIGNMENT.....	6
4.0 ELECTRICALSPECIFICATIONS.....	7
5.0 OPTICAL CHARACTERISTICS.....	18
6.0 RELIABILITY TEST ITEM.....	21
7.0 PRECAUTIONSr.....	22
8.0PACKAGE SPECIFICATION.....	27

1.0 GENERAL DESCRIPTION

1.1 Introduction

This module is a color active matrix LCD module incorporating Oxide TFT (Thin Film Transistor).It is composed of a color TFT-LCD panel, driver ICs, a control circuit and power supply circuit. Graphics and texts can be displayed on a 1920×3 (RGB)×1080 dots panel with 262144(6 bit) colors by using eDP (Embedded Display Port) Ver1.2 interface and supplying +3.3V DC supply voltage for TFT-LCD panel driving.

In this TFT-LCD panel, color filters for excellent color performance is incorporated to realize brighter and clearer pictures, making this Module optimum for use in multi-media applications.

Optimum viewings are in all directions.

10serial-4parallel LED structure.

Backlight-driving LED controller is built in this Module.

This module is capable to support SDRRS(Default as enable) / SSC(Default as disable).

This module do not support PSR/MBO/NVSR/G-Sync features.

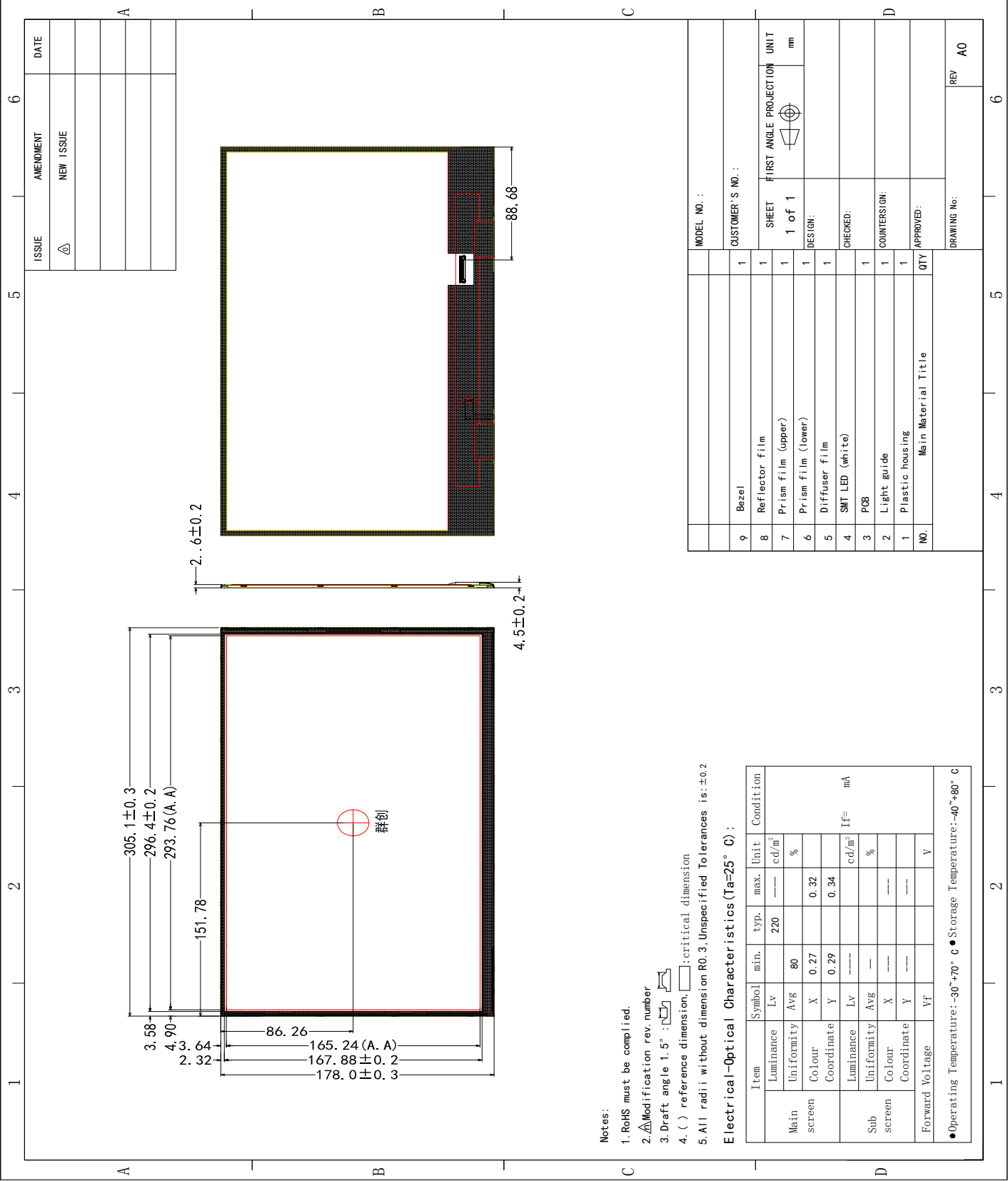
1.2General information

No.	Item	Specification	Unit
1	Panel Size	13.3”	inch
2	Number of Pixels	1920XRGB(3)X1080	pixels
3	Active Area	293.76(H) × 165.24(V)	mm
4	Pixel Pitch	0.153(H) x 0.153 (V)	mm
5	Outline Dimension	305.1 (H)*178(V)*2.6(D)	mm
6	Number of Colors	262.144	-
7	Display Mode	Normally Black	-
8	Display Format	RGB vertical stripe	-
9	Luminance (cd/m ²)	220(TYP.)	nit
10	Interface	eDP	-
11	Backlight	White LED	-
12	Operation Temperature	0~50	℃
13	Storage Temperature	-20~60	℃
14	Weight	TBD	g

Outline dimensions

Parameter		Min.	Typ.	Max.	Unit	Remark
Unit outline dimensions	Width	304.8	305.1	305.4	mm	
	Height	177.7	178	178.3	mm	
	Depth	2.4	2.6	2.8	mm	
Mass			TBD		g	with protect films

2.0 MECHANICAL SPECIFICATION



3.INPUT INTERFACE PIN ASSIGNMENT

3-1 Driving interface of PWB

Pin No.	Symbol	I/O	Function	Remark
1	NC	-	Reserved for LCD	[Note3-1-1]
2	H_GND	P	High Speed Ground	
3	Lane1_N	I	Complement Signal Link Lane 1	
4	Lane1_P	I	True Signal Link Lane 1	
5	H_GND	P	High Speed Ground	
6	Lane0_N	I	Complement Signal Link Lane 0	
7	Lane0_P	I	True Signal Link Lane 0	
8	H_GND	P	High Speed Ground	
9	AUX_CH_P	I	True Signal Auxiliary Channel	
10	AUX_CH_N	I	Complement Signal Auxiliary Channel	
11	H_GND	P	High Speed Ground	
12	LCD_VDD	P	LCD logic and driver power(3.3V)	
13	LCD_VDD	P	LCD logic and driver power(3.3V)	
14	NC	I	Reserved for LCD manufacturer's use	[Note3-1-1]
15	LCD_GND	P	LCD logic and driver ground	
16	LCD_GND	P	LCD logic and driver ground	
17	HPD	O	HPD signal pin	[Note3-1-2]
18	BL_GND	P	Backlight ground	
19	BL_GND	P	Backlight ground	
20	BL_GND	P	Backlight ground	
21	BL_GND	P	Backlight ground	
22	BL_ENABLE	I	Backlight ON/OFF	[Note3-1-3]
23	BL_PWM_DIM	I	System PWM	[Note3-1-4]
24	NC	-	Reserved for LCD manufacturer's use	[Note3-1-1]
25	NC	-	Reserved for LCD manufacturer's use	[Note3-1-1]
26	BL_PWR	P	Backlight power	
27	BL_PWR	P	Backlight power	
28	BL_PWR	P	Backlight power	
29	BL_PWR	P	Backlight power	
30	NC	-	Reserved for LCD manufacturer's use	[Note3-1-1]

*1 P: POWER I: Input O: Output

The shielding case is connected with signal GND

- Connector used :20455-030E-76 (I-PEX)
- Corresponding connector : 20453-030T (I-PEX)

(Panda is not responsible to its product quality, if the user applies a connector not corresponding to the above model.)

All terminals except NC terminal must be connected to input signal described as above or supply voltage or GND each

4.0 ELECTRICAL SPECIFICATIONS

4.1 LCD ELETRONICS SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)(7)
HPD	High Level		2.25	-	2.75	V	(6)
	Low Level		0	-	0.4	V	(6)
HPD Impedance		R _{HPD}	30K			ohm	(5)
Ripple Voltage		V _{RP}	-	-	100	mV	(1)
CE_EN Input Voltage	High Level	V _{IHCE}	2.3	-	3.6	V	(5)
	Low Level	V _{ILCE}	0	-	0.5	V	(5)
CE_EN Impedance		R _{CE_EN}	30K	-	-	ohm	(5)
CABC_EN Input Voltage	High Level	V _{IHCABC}	2.3	-	3.6	V	(5)
	Low Level	V _{ILCABC}	0	-	0.5	V	(5)
CABC_EN Impedance		R _{CABC_EN}	30K	-	-	ohm	(5)
Inrush Current		I _{RUSH}	-	-	1.5	A	(1),(2)
Power Supply Current	Mosaic	I _{CC}	-	(121)	(133)	mA	(3)a
	Black		-	(121)	(133)	mA	(3)
Power per EBL WG		P _{EBL}	-	(0.75)	-	W	(4)

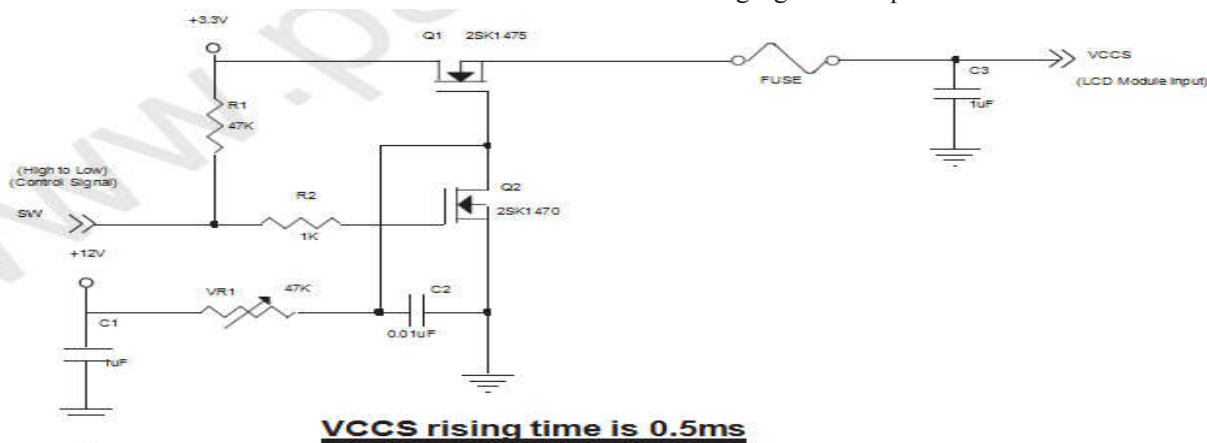
Note (1) The ambient temperature is $T_a = 25$

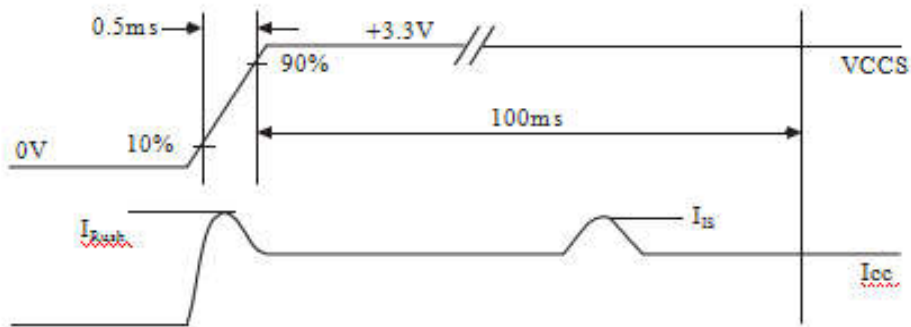
± 2 °C. Note (2) I_{RUSH}: the maximum current

when VCCS is rising

I_S: the maximum current of the first 100ms after power-on

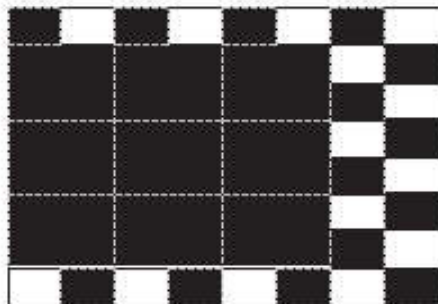
Measurement Conditions: Shown as the following figure. Test pattern: black.





Note (3) The specified power supply current is under the conditions at $V_{CCS} = 3.3\text{ V}$, $T_a = 25 \pm 2^\circ\text{C}$, DC Current and $f_v = 60\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. Mosaic Pattern



Active Area

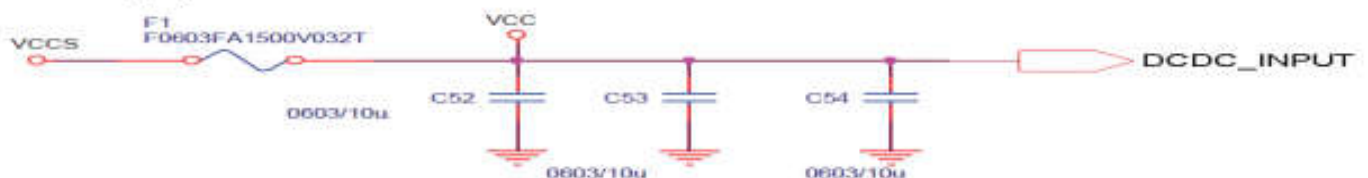
Note (4) The specified power are the sum of LCD panel electronics input power and the converter input power. Test conditions are as follows.

- (a) $V_{CCS} = 3.3\text{ V}$, $T_a = 25 \pm 2^\circ\text{C}$, $f_v = 60\text{ Hz}$,
- (b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.
- (c) Luminance: 60 nits

Note (5) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. Please refer to Note (4) of 4.3.2 LED CONVERTER SPECIFICATION to obtain more information.

Note (6) When a source detects a low-going HPD pulse, it must be regarded as a HPD event. Thus, the source must read the link / sink status field or receiver capability field of the DPCD and take corrective action

Note (7) Input VCC Circuit is as below



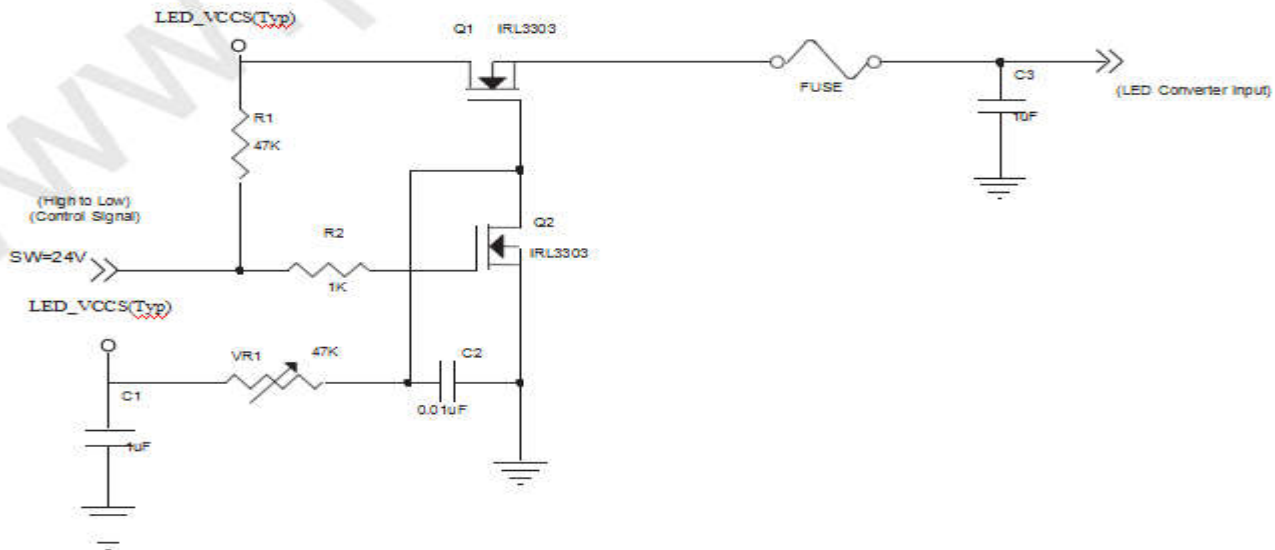
4.2LED CONVERTER SPECIFICATION

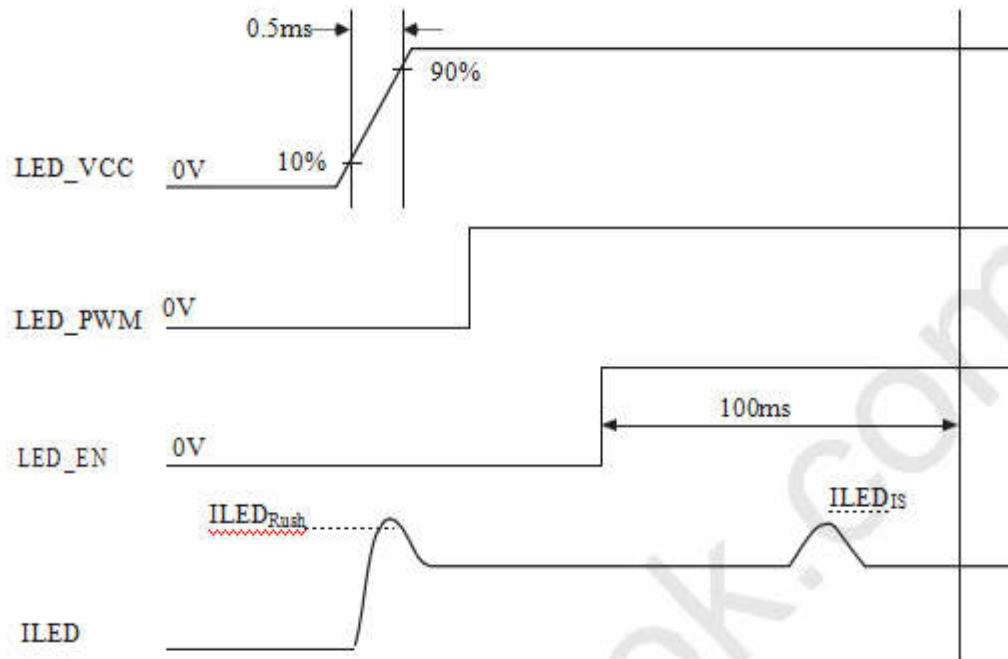
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input power supply voltage		LED_Vccs	5	12	21	V	
Converter Inrush Current		I _{LED_RUSH}	-	-	1.5	A	(1)
EN Control Level	Backlight On		2.2	-	3.6	V	(4)
	Backlight Off		0	-	0.6	V	(4)
LED_EN Impedance		R _{LED_EN}	30K	-	-	ohm	(4)
PWM Control Level	PWM High Level		2.2	-	3.6	V	(4)
	PWM Low Level		0	-	0.6	V	(4)
PWM Impedance		R _{PWM}	30K	-	-	ohm	(4)
PWM Control Duty Ratio			5	-	100	%	(5)
PWM Control Permissive Ripple Voltage		V _{PWM_pp}	-	-	100	mV	
PWM Control Frequency		f _{PWM}	190	-	2K	Hz	(2)
LED Power Current	LED_VCCS =Typ.		(105)	(123)	(129)	mA	(3)

Note (1) I_{LED_RUSH}: the maximum current when LED_VCCS is rising,

I_{LED_IS}: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 °C, 200 Hz, Duty=100%.





Note (2) If PWM control frequency is applied in the range less than 1KHz, the “waterfall” phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

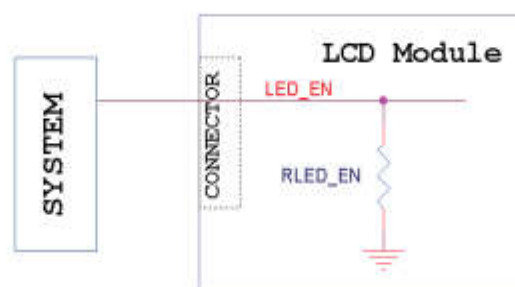
PWM control frequency f_{PWM} should be in the range

$$(N + 0.33) \times f \leq f_{PWM} \leq (N + 0.66) \times f$$

N : Integer ($N \geq 3$)
 f : Frame rate

Note (3) The specified LED power supply current is under the conditions at “LED_VCCS = Typ.”, $T_a = 25 \pm 2^\circ\text{C}$, $f_{PWM} = 200\text{ Hz}$, Duty=100%.

Note (4) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. For example, the figure below describes the equivalent pull down impedance of LED_EN (If it exists). The rest pull down impedances of other signals (eg. HPD, PWM ...) are in the same concept.

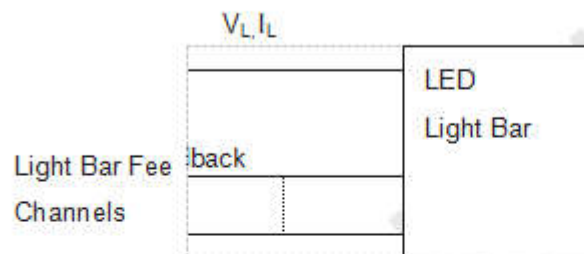


Note (5) If the cycle-to-cycle difference of PWM duty exceeds 0.1%, especially when the PWM duty is low, slight brightness change might be observed.

4.3BACKLIGHT UNIT

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V_L	26.0	28.0	30.0	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	I_L	(47)			mA	
Power Consumption	P_L	-	(1.216)	(1.410)	W	(3)
LED Life Time	L_{BL}	15000	-	-	Hrs	(4)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below :



Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

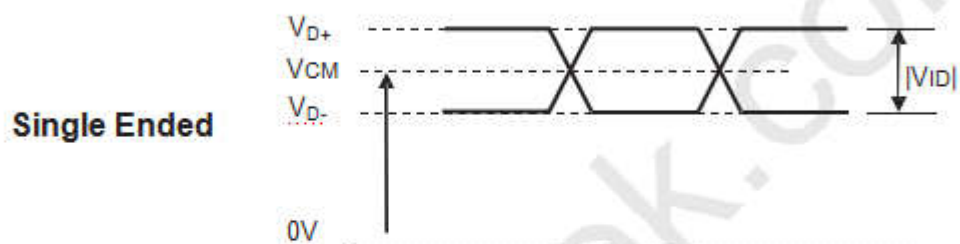
Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at $T_a = 25 \pm 2^\circ\text{C}$ and $I_L = (9.4) \text{ mA}$ (Per EA) until the brightness becomes 50% of its original value.

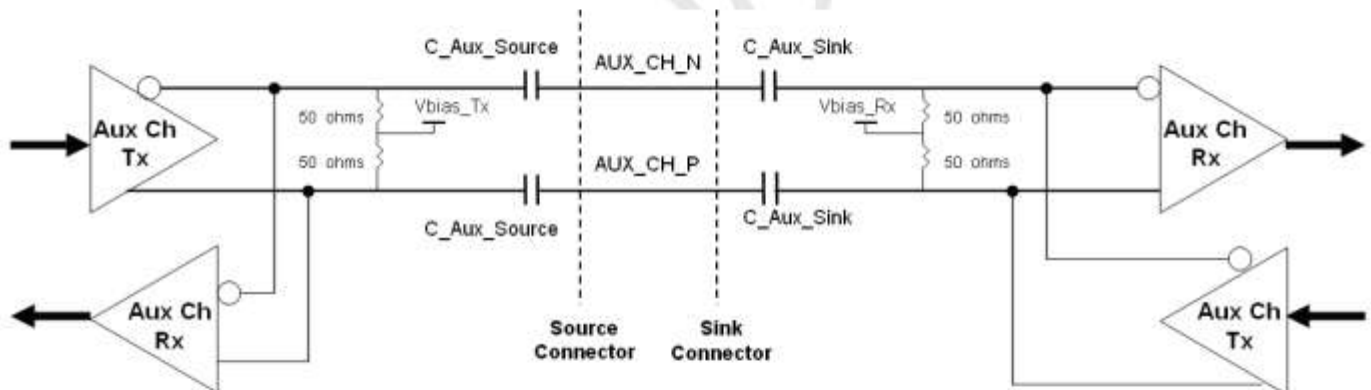
4.4 DISPLAY PORT INPUT SIGNAL TIMING SPECIFICATIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Differential Signal Common Mode Voltage(MainLink and AUX)	VCM	0		2	V	(1)(4)
AUX AC Coupling Capacitor	C_Aux_Source	75		200	nF	(2)
Main Link AC Coupling Capacitor	C_ML_Source	75		200	nF	(3)

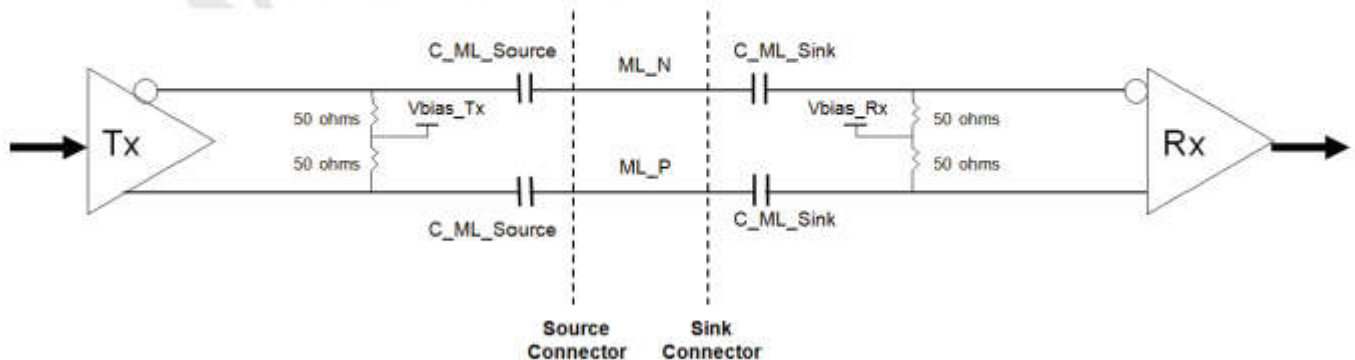
Note (1) Display port interface related AC coupled signals should follow VESA DisplayPort Standard Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.2. There are many optional items described in eDP1.3. If some optional item is requested, please contact us.



(2) Recommended eDP AUX Channel topology is as below and the AUX AC Coupling Capacitor (C_Aux_Source) should be placed on the source device.



(3) Recommended Main Link Channel topology is as below and the Main Link AC Coupling Capacitor (C_ML_Source) should be placed on the source device.



(4) The source device should pass the test criteria described in DisplayPort Compliance Test Specification (CTS) 1.1

4.4.2 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(61)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Green(63)																		
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
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	:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Blue(63)																		

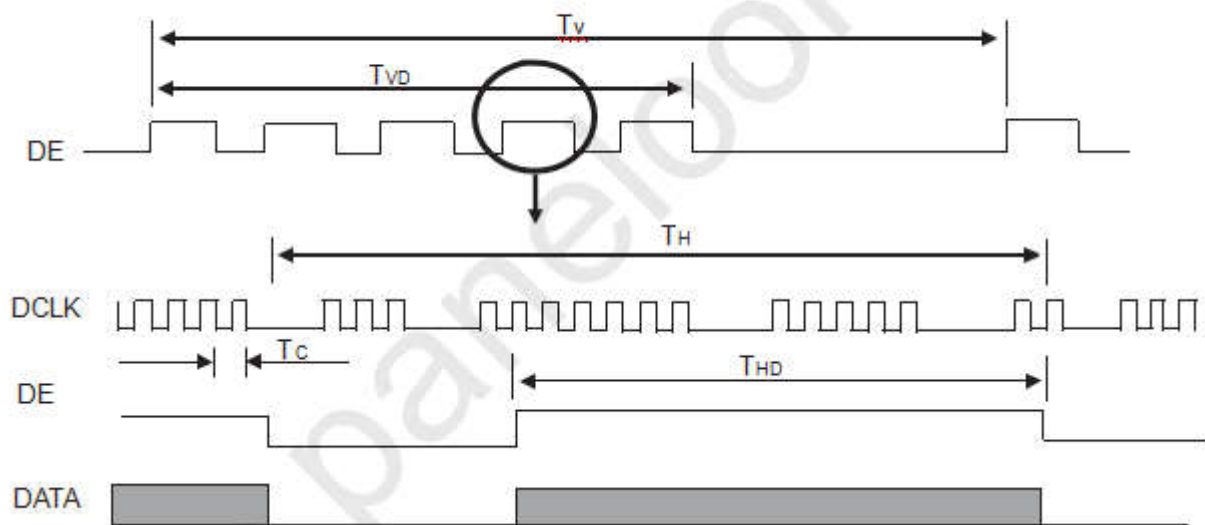
4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

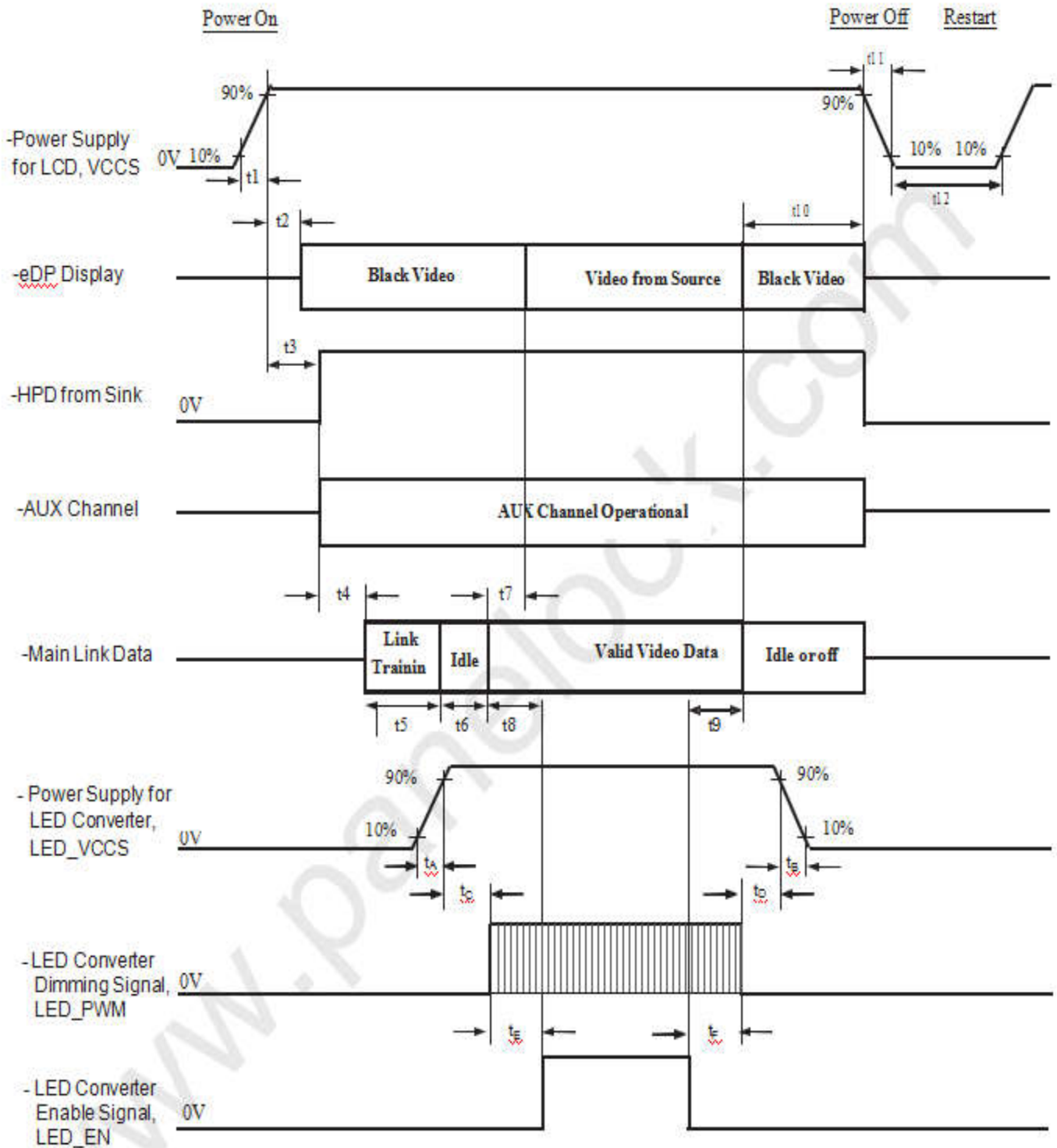
Refresh Rate 60Hz

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	152.08	152.84	153.6	MHz	-
DE	Vertical Total Time	TV	1128	1132	1136	TH	-
	Vertical Active Display Period	TVD	1080	1080	1080	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	52	TV-TVD	TH	-
	Horizontal Total Time	TH	2230	2250	2270	Tc	-
	Horizontal Active Display Period	THD	1920	1920	1920	Tc	-
	Horizontal Active Blanking Period	THB	TH-THB	330	TH-THB	Tc	-

INPUT SIGNAL TIMING DIAGRAM



4.6 POWER ON/OFF SEQUENCE



Timing Specifications (TBD)

Parameter	Description	Reqd. By	Value		Unit	Notes
			Min	Max		
t1	Power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t2	Delay from LCD,VCCS to black video generation	Sink	0	200	ms	Automatic Black Video generation prevents display noise until valid video data is received from the Source (see Notes:2 and 3 below)
t3	Delay from LCD,VCCS to HPD high	Sink	0	200	ms	Sink AUX Channel must be operational upon HPD high (see Note:4 below)
t4	Delay from HPD high to link training initialization	Source	0	-	ms	Allows for Source to read Link capability and initialize
t5	Link training duration	Source	0	-	ms	Dependant on Source link training protocol
t6	Link idle	Source	0	-	ms	Min Accounts for required BS-Idle pattern. Max allows for Source frame synchronization
t7	Delay from valid video data from Source to video on display	Sink	0	50	ms	Max value allows for Sink to validate video data and timing. At the end of T7, Sink will indicate the detection of valid video data by setting the SINK_STATUS bit to logic 1 (DPCD 00205h, bit 0), and Sink will no longer generate automatic Black Video
t8	Delay from valid video data from Source to backlight on	Source	80	-	ms	Source must assure display video is stable *: Recommended by INX. To avoid garbage image.
t9	Delay from backlight off to end of valid video data	Source	50	-	ms	Source must assure backlight is no longer illuminated. At the end of T9, Sink will indicate the detection of no valid video data by setting the SINK_STATUS bit to logic 0 (DPCD 00205h, bit 0), and Sink will automatically display Black Video. (See Notes: 2 and 3 below) *: Recommended by INX. To avoid garbage image.

t10	Delay from end of valid video data from Source to power off	Source	0	500	ms	Black video will be displayed after receiving idle or off signals from Source
t11	VCCS power rail fall time, 90% to 10%	Source	0.5	10	ms	-

t12	VCCS Power off time	Source	500	-	ms	-
t _A	LED power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t _B	LED power rail fall time, 90% to 10%	Source	0	10	ms	-
t _C	Delay from LED power rising to LED dimming signal	Source	1	-	ms	-
t _D	Delay from LED dimming signal to LED power falling	Source	1	-	ms	-
t _E	Delay from LED dimming signal to LED enable signal	Source	0	-	ms	-
t _F	Delay from LED enable signal to LED dimming signal	Source	0	-	ms	-

Please don't plug or unplug the interface cable when system is turned on.

Note (2) The Sink must include the ability to automatically generate Black Video autonomously. The Sink must automatically enable Black Video under the following conditions:

- Upon LCDVCC power-on (within T2 max)

- When the "NoVideoStream_Flag" (VB-ID Bit 3) is received from the Source (at the end of T9)

Note (3) The Sink may implement the ability to disable the automatic Black Video function, as described in Note (2), above, for system development and debugging purposes.

Note (4) The Sink must support AUX Channel polling by the Source immediately following LCDVCC power-on without causing damage to the Sink device (the Source can re-try if the Sink is not ready). The Sink must be able to response to an AUX Channel transaction with the time specified within T3 max.

5.OPTICAL CHARACTERISTICS

5.1TEST CONDITIONS

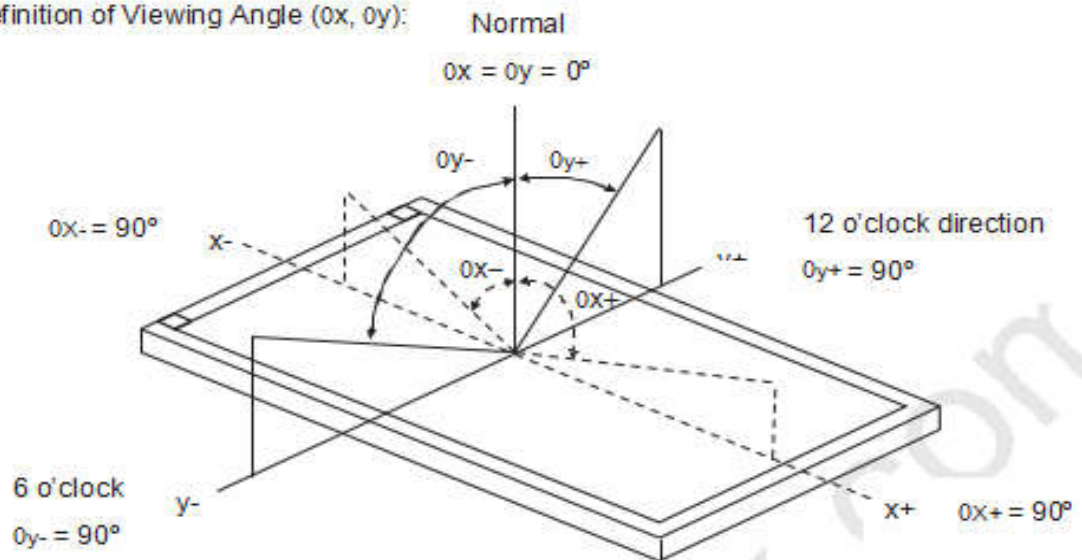
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V _{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I _L	(47)	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note					
Contrast Ratio		CR	0 _x =0°, 0 _y =0° Viewing Normal Angle	800	1000	-	-	(2), (5) ,(7)					
Response Time		T _R		-	14	19	ms	(3) ,(7)					
		T _F		-	11	16	ms						
Average Luminance of White		L _{Ave}		Typ – 0.03	300	300	-	cd/m ²	(4), (6) ,(7)				
Color Chromaticity	Red	R _x								0.640	Typ + 0.03	-	(1) ,(7)
		R _y								0.330		-	
	Green	G _x								0.300		-	
		G _y								0.600		-	
	Blue	B _x								0.150		-	
		B _y								0.060		-	
	White	W _x								0.313		-	
		W _y								0.329		-	
Viewing Angle	Horizontal	0 _x +	CR□10							80	85	-	Deg.
		0 _x -		80	85	-							
	Vertical	0 _y +		80	85	-							
		0 _y -		80	85	-							
White Variation		6W _{5p}	0 _x =0°, 0 _y =0°	-	1.11	1.25	-	(5),(6) , (7)					
		6W _{13p}	0 _x =0°, 0 _y =0°	-	1.34	1.54	-						

Note (1) Definition of Viewing Angle (θ_x, θ_y):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{63} / L_0$$

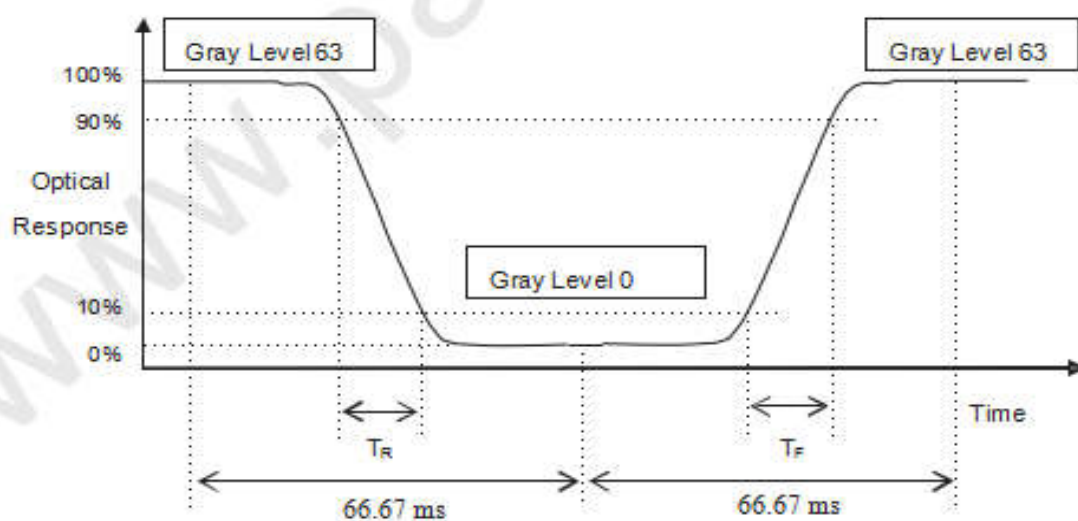
L_{63} : Luminance of gray level 63

L_0 : Luminance of gray level 0

$$CR = CR(1)$$

$CR(X)$ is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

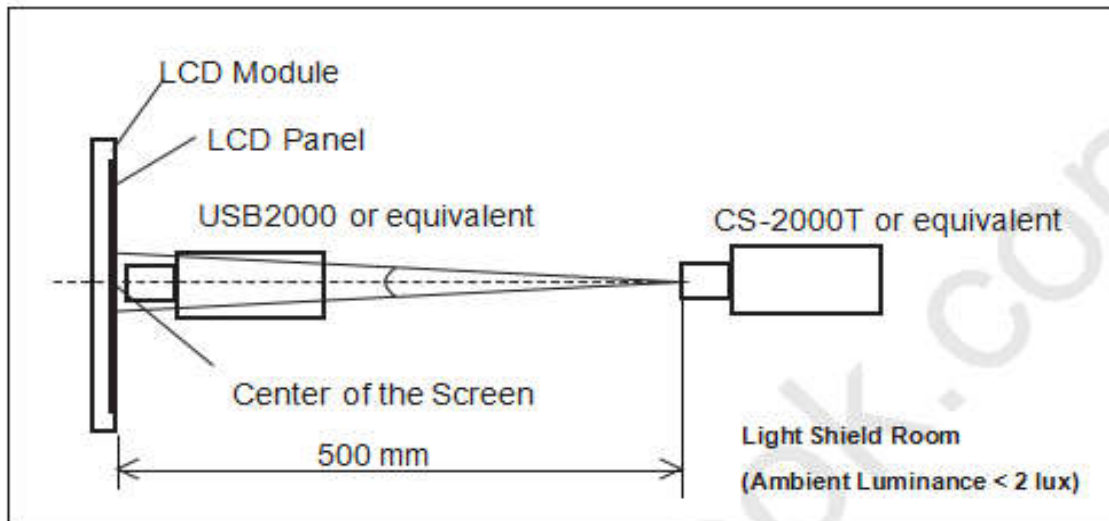
Measure the luminance of gray level 63 at 5 points

$$L_{AVE} = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$$

$L(X)$ is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

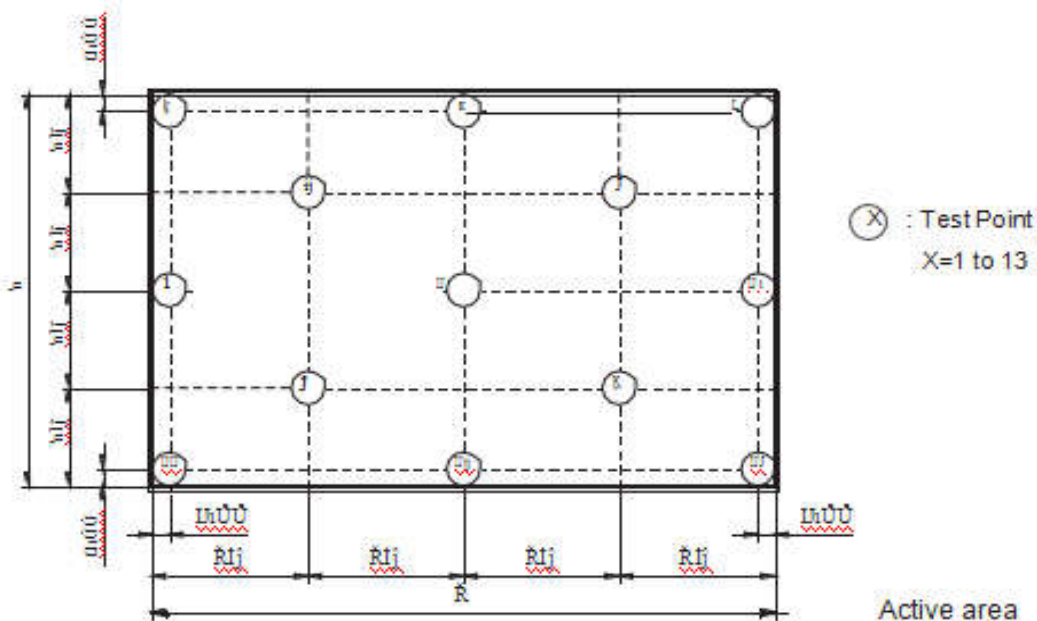


Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 5 points

$$\delta W_{5p} = \text{Maximum} [L(1) \quad L(5)] / \text{Minimum} [L(1) \quad L(5)]$$

$$\delta W_{13p} = \text{Maximum} [L(1) \quad L(13)] / \text{Minimum} [L(1) \quad L(13)]$$



Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

6.RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	60°C, 240 hours	(1) (2)
Low Temperature Storage Test	-20°C, 240 hours	
Thermal Shock Storage Test	-20°C, 0.5hour←→60d, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	50°C, 240 hours	
Low Temperature Operation Test	0°C, 240 hours	
High Temperature & High Humidity Operation Test	50°C, RH 80%, 240hours	
ESD Test (Operation)	150pF, 330Ω, 1sec/cycle Condition 1 : Contact Discharge, ±8KV Condition 2 : Air Discharge, ±15KV	(1)
Shock (Non-Operating)	220G, 2ms, half sine wave, 1 time for each direction of ±X, ±Y, ±Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

Note (1) criteria : Normal display image with no obvious non-uniformity and no line defect. Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

7.PRECAUTIONS

7.1HANDLING PRECAUTIONS

- (1)The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.
- (2)While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.
- (3)Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (4)Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.
- (5)If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.
- (6)Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.
- (7)If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8)Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.
- (9)Do not disassemble the module.
- (10)Do not pull or fold the LED wire.
- (11)Pins of I/F connector should not be touched directly with bare hands.

7.2STORAGE PRECAUTIONS

- (1)High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (2)It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.
- (3)It may reduce the display quality if the ambient temperature is lower than 10 °C. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

7.3OPERATION PRECAUTIONS

- (1)Do not pull the I/F connector in or out while the module is operating.
- (2)Always follow the correct power on/off sequence whe

Appendix. EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPD standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	ID system manufacturer name ("CMN")	0D	00001101
9	9	ID system manufacturer name	AE	10101110
10	0A	ID system Product Code (LSB)	90	10010000
11	0B	ID system Product Code (MSB)	13	00010011
12	0C	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
13	0D	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
14	0E	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
15	0F	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
16	10	Week of manufacture (fixed week code)	10	00010000
17	11	Year of manufacture (fixed year code)	1C	00011100
18	12	Version=1	01	00000001
19	13	Revision=4	04	00000100
20	14	Vedio Input Definition	95	10010101
21	15	Active area horizontal ("29.376cm")	1D	00011101
22	16	Active area vertical ("16.524cm")	11	00010001
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support ("RGB, Non-continous")	02	00000010
25	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	EE	11101110
26	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	95	10010101
27	1B	Rx=0.64	A3	10100011
28	1C	Ry=0.33	54	01010100
29	1D	Gx=0.3	4C	01001100
30	1E	Gy=0.6	99	10011001
31	1F	Bx=0.15	26	00100110
32	20	By=0.06	0F	00001111
33	21	Wx=0.313	50	01010000

34	22	Wy=0.329	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	No manufacturer's specific timing	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001

42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock ("152.84MHz")	B4	10110100
55	37	# 1 Pixel clock (hex LSB first)	3B	00111011
56	38	# 1 H active ("1920")	80	10000000
57	39	# 1 H blank ("330")	4A	01001010
58	3A	# 1 H active : H blank	71	01110001
59	3B	# 1 V active ("1080")	38	00111000
60	3C	# 1 V blank ("52")	34	00110100
61	3D	# 1 V active : V blank	40	01000000
62	3E	# 1 H sync offset ("48")	30	00110000
63	3F	# 1 H sync pulse width ("32")	20	00100000
64	40	# 1 V sync offset : V sync pulse width ("3 : 5")	35	00110101
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width	00	00000000
66	42	# 1 H image size ("293 mm")	25	00100101
67	43	# 1 V image size ("165 mm")	A5	10100101
68	44	# 1 H image size : V image size	10	00010000
69	45	# 1 H boarder ("0")	00	00000000
70	46	# 1 V boarder ("0")	00	00000000
71	47	Non-interlaced, Normal Display, Digital separate, Positive Hsync, Negative Vsync	1A	00011010

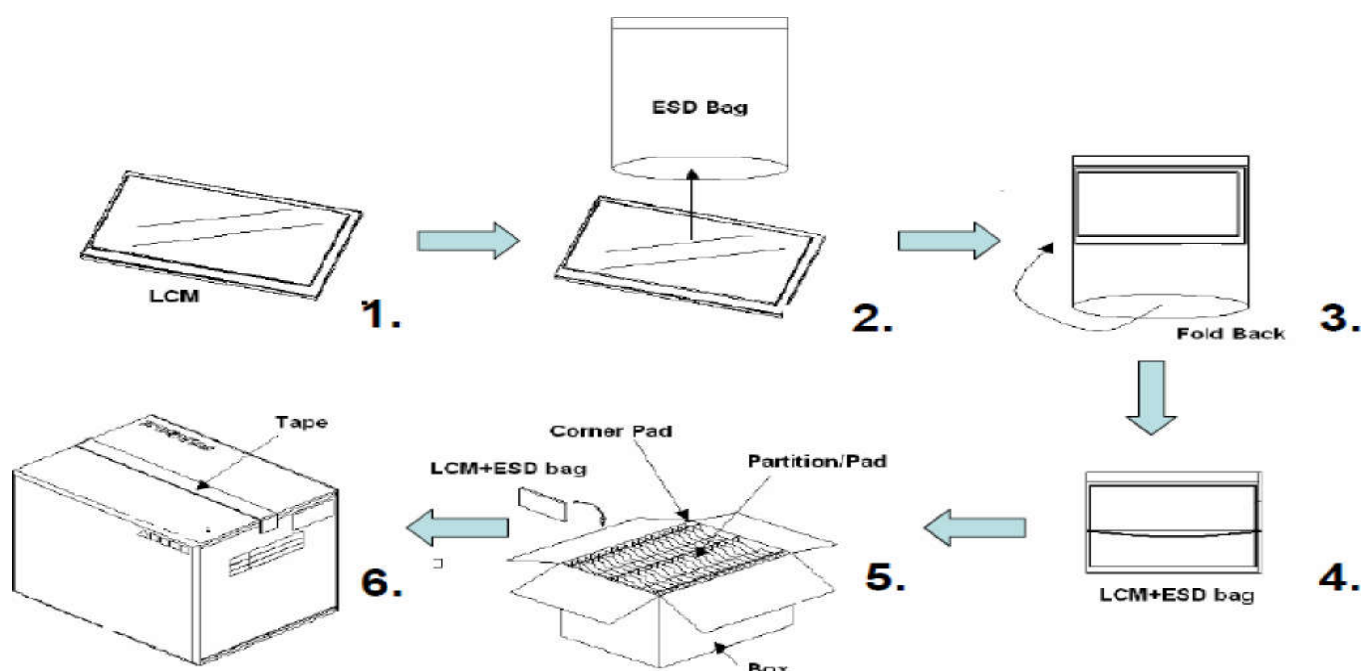
72	48	Detailed timing description # 2 Pixel clock ("152.84MHz")	B4	10110100
73	49	# 2 Pixel clock (hex LSB first)	3B	00111011
74	4A	# 2 H active ("1920")	80	10000000
75	4B	# 2 H blank ("330")	4A	01001010
76	4C	# 2 H active : H blank	71	01110001
77	4D	# 2 V active ("1080")	38	00111000
78	4E	# 2 V blank ("335")	4F	01001111
79	4F	# 2 V active : V blank	41	01000001
80	50	# 2 H sync offset ("48")	30	00110000
81	51	# 2 H sync pulse width ("32")	20	00100000
82	52	# 2 V sync offset : V sync pulse width ("3 : 5")	35	00110101
83	53	# 2 H sync offset : H sync pulse width : V sync offset : V sync width	00	00000000
84	54	# 2 H image size ("293 mm")	25	00100101
85	55	# 2 V image size ("165 mm")	A5	10100101
86	56	# 2 H image size : V image size	10	00010000
87	57	# 2 H boarder ("0")	00	00000000

88	58	# 2 V boarder ("0")	00	00000000
89	59	Non-interlaced, Normal Display, Digital separate, Positive Hsync, Negative Vsync	1A	00011010
90	5A	Flag	00	00000000
91	5B	Flag	00	00000000
92	5C	Flag	00	00000000
93	5D	Data Type Tag: Alphanumeric Data String (ASCII)	FE	11111110
94	5E	Flag	00	00000000
95	5F	Dell P/N 1st Character "M"	4D	01001101
96	60	Dell P/N 2nd Character "F"	46	01000110
97	61	Dell P/N 3rd Character "9"	39	00111001
98	62	Dell P/N 4th Character "5"	35	00110101
99	63	Dell P/N 5th Character "F"	46	01000110
100	64	EDID Revision	00	00000000
101	65	Manufacturer P/N "1"	31	00110001
102	66	Manufacturer P/N "3"	33	00110011
103	67	Manufacturer P/N "3"	33	00110011
104	68	Manufacturer P/N "H"	48	01001000
105	69	Manufacturer P/N "C"	43	01000011
106	6A	Manufacturer P/N "G"	47	01000111
107	6B	New line character indicates end of ASCII string	0A	00001010
108	6C	Flag	00	00000000
109	6D	Flag	00	00000000

110	6E	Flag	00	00000000
111	6F	Data Type Tag: Manufacturer Specified Data 00	00	00000000
112	70	Flag	00	00000000
113	71	Color Management	00	00000000
114	72	Panel Type and Revision	41	01000001
115	73	Frame Rate	01	00000001
116	74	Light Controller Interface and Maximum Luminance	9E	10011110
117	75	Front Surface / Polarizer and Pixel Structure	00	00000000
118	76	Multi-Media Features	10	00010000
119	77	Multi-Media Features	00	00000000
120	78	Special Features	00	00000000
121	79	Special Features	0A	00001010
122	7A	Special Features	01	00000001
123	7B	New line character indicates end of ASCII string	0A	00001010
124	7C	Padding with "Blank" character	20	00100000
125	7D	Padding with "Blank" character	20	00100000
126	7E	No extension	00	00000000
127	7F	Checksum	3B	00111011

8.0 PACKAGE SPECIFICATION

LCM Model	LCM Qty. in the box	Inner Box Size (mm)	Notice
KQ13304HI30-50A	30 pcs/box		



Items	Material	Notice
Box	Corrugated Paper Board	AB Flute
Partition/Pad	Corrugated Paper Board	B Flute
Corner Pad	Corrugated Paper Board	AB Flute
ESD bag	PE	